Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	34	(clock adj buffer) same (dummy adj load)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/27 10:30
L2	0	(clock adj buffer) same (dummy adj load) same (wiring adj layer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/27 10:31
L3	0	(clock adj buffer) same (dummy adj load) same (wire adj layer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/27 10:32
L4	0	(buffer) same (dummy adj load) same (wiring adj layer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/27 10:32
S1	985	716/12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/27 10:28
S2	284	716/15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 14:54
S3	0	(716/12).ccls. and ((wiring adj layer) adj switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:05
S4	0	(716/15).ccls. and ((wiring adj layer) adj switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:06
S5	1	("716"/$).ccls. and ((wiring adj layer) adj switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:07
S6	1382	716/6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:07

S7	1	(716/6).ccls. and ((wiring adj layer) adj switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:07
S8	24	((wiring adj layer) adj switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 18:28
S9	2674	((wiring adj layers) and switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:41
S10	15	((wiring adj layers) adj switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 15:55
S11	385	((wiring adj layers) same switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 16:30
S12	47	(clock adj wiring $2) and (two adj (wiring adj layers)) and ((wiring adj layers) same switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 17:18
S13	45	((wiring adj layers) same via same switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/20 18:28
S14	1	((clock adj wiring$2) near switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/21 10:23
S15	33	((clock adj wiring$2) same switch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/21 10:41
S16	1	((clock adj buffer$2) and (clock adj wiring$2) and (wiring adj layers) and switch$4).CLM.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/21 10:42

S17	2	(antenna adj effect) and (clock adj tree)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 15:37
S18	99	(antenna adj effect) and (clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 15:38
S19	16	(antenna adj effect) same (clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 15:46
S20	8	(antenna adj effect) same (metal adj layers)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 15:48
S21	23	(antenna adj effect) same (metal same wiring)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/09/22 15:49